ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Stacking Memory Chips Using Flat Lead-Frame with Breakaway Insertion Pins and Pin-to-Pin Bridges

Application Number :

Confirmation Number:

First Named Applicant: Ren-Kang Chiou

Attorney Docket Number: ML-17

Art Unit:

Examiner:

Search string: (6617673 or 6603196 or 6566760 or 6542393 or 6521993 or 6388336 or 6307256 or 6028352 or 5780925 or 5677569 or 5587341 or 5490041 or 5434745 or 5138438 or 4884237 or 4743956).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
WB	1	6617673	2003-09-09	Lee , et al.	B1	257	676
WB	2	6603196	2003-08-05	Lee , et al.	B1	257	676
WB	3	6566760	2003-05-20	Lee , et al.	B1	257	777
WB	4	6542393	2003-04-01	Chu , et al.	B1	365	51
WB	5	6521993	2003-02-18	Masayuki , et al.	B1	257	723
WB	6	6388336	2002-05-14	Venkateshwaran , et al.	B1	257	779
WB	7	6307256	2001-10-23	Chiang , et al. .	B1	257	668
WB	8	6028352	2000-02-22	Eide	B1	257	686
WB	9	5780925	1998-07-14	Eide	B1	257	676
WB	10	5677569	1997-10-14	Choi , et al.	B1	257	686
WB	11	5587341	1996-12-24	Masayuki , et al.	B1	438	109
WB	12	5490041	1996-02-06	Furukawa , et al.	B1	361	777
WB	13	5434745	1995-07-18	Shokrgozar , et al.	B1	361	735
WB	14	5138438	1992-08-11	Masayuki , et al.	B1	257	686
WB	15	4884237	1989-11-28	Mueller , et al.	B1	365	63
WB	16	4743956	1988-05-10	Olla , et al.	B1	257	674

Signature

Examiner Name	Date
William. Baumeister	19 MAR 05